The Merrimac streaming supercomputer project aims to develop a scientific computer that offers an order of magnitude or more improvement in performance per unit cost compared to cluster-based scientific computers built from the same underlying semiconductor and packaging technology. We expect this efficiency to arise from two innovations: stream architecture and advanced interconnection networks. Organizing the computation into streams and exploiting the resulting locality using a register hierarchy enables a stream architecture to reduce the memory bandwidth required by representative computations by an order of magnitude or more.

Requirements for Achieving High Performance on Modern Semiconductor Processes

- Parallelism: 100 GFLOPS per chip (millions per system)
- Latency Tolerance: 500 cycle remote memory access
- Locality: To match 20Gbps/ALU bandwidth to ~100Gbps/chip bandwidth

Merrimac Architecture

- 90nm CMOS process (1 V)
- ASIC technology
- 1 GHz (37 FO4)
- 128 GFLOPs

Merrimac Node

- Inter-cluster switch between clusters
- 156.25 mm² (small ~12.5 x 12.5)
- Stanford Imagi is 16mm x 16mm
- MIT Raw is 18mm x 18mm
- 25 Watts per processor (P4 = 75 W)
- 41 Watts total per node (with DRAM)

Memory System

- Single instruction accesses thousands of multi-word records
- Fill a very deep and wide memory pipeline
- High-performance bandwidth
  - 16 banks of 1 Gbit DDR2-SDRAM for 25.6 GBytes peak memory bandwidth
  - Memory access scheduling
  - Improves average DRAM bandwidth
  - Bandwidth amplification through stream cache
- High bandwidth global memory space
  - Flat address space to access local memory at any node
  - Segregate registers translate virtual addresses
  - Network controller performs remote accesses
  - High radix routers allow for efficient single word messages

Stream Register File

- Single ported memory
  - Efficient wide access of 4 contiguous words
- Implemented using sub-arrays
  - Reduced access time
  - Reduced power
- Stream-buffers match bandwidth to compute needs
  - Time multiplex the SRF port
- Indexed SRF at low extra cost
  - 8:1 MUX in sub-arrays
  - Row decoder per sub-array

Iterative Unit

- Speeds up inverse and inverse sqrt
  - Generates 27 bits of precision
- Newton-Raphson iteration
  - on MADD units

Merrimac Node

- Clocks: 100 MHz
- Power: 200W

Merrimac System

- 32 boards
- Bandwidth: 256GB/s
- Memory: 4GB
- DRAM: 128GB
- Clocks: 100 MHz
- Power: 200W

Merrimac Implementation Plan

- Completed Merrimac processor architecture specification document
- Architecture definition, instruction set architecture. Exceptions
  - Responded to NASA HARP BAA with detailed prototype plan
- Chip design steps (in collaboration with LLNL):
  - Contact several chip design firms for accurate estimates and design proposals
  - Chip design with most competitive firm
  - Fabrication, testing and packaging
- System design steps (in collaboration with LLNL):
  - Merrimac processors designed to integrate with Cray XARC interconnection network
  - Merrimac boards designed to plug into Cray Rainer system
- Software system steps:
  - Continued compiler development collaboration with Reservoir Labs
  - Collaborate with LLNL on run-time system design
  - Collaborate with LBNL on UPC integration and multi-node

Status: October 2004